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INDUSTRY INSIGHTS

Moore's Law — the z dimension

Moore's Law currently states that the number of circuit functions on the surface of a chip doubles approximately every two years. Although simple miniaturization in the *x-y* plane ("shrinks") has traditionally resulted in increased functional integration, the cost and complexity of pushing this process forward is escalating. Also, advances in individual chip performance are becoming increasingly irrelevant due to performance bottlenecks in chip-to-chip interconnection. The costs of "real-estate" on a silicon chip and a printed circuit board are reaching a point where future functional integration may best occur in the vertical (z) dimension. It is likely that, unless we shift focus toward affordable, vertical miniaturization and integration, further investment in reducing feature size will generate diminishing returns. We need to shift Moore's Law to 3-D for further advances in the 21st century.

2.5-D chip stacking

Chip stacking inside a thin small outline package (TSOP) has been in production since 1995. This is often referred to as a 2.5-D wire-bonding package. It's smaller than a 2-D printed circuit board assembly, but not as complex as a true 3-D package. With relatively small investment, many companies have already started using 2.5-D stacking technologies to gain the *x-y* area space benefits for mobile communications and hand-held computing applications. Recently, Sharp, Mitsubishi, Hitachi, and Intel agreed to standardize specifications for wire-bonded, stacked, chip-scale packages (S-CSP) as multiple memory modules. In addition, five other packaging and assembly companies, Seiko, Sanyo, Mitsui, Amkor, and Power Technology, have said they will support the unified S-CSP specifications.

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Vertical stacking of multiple chips in the same package has been expensive to achieve because all known production techniques occurred at the die rather than the wafer level.

Vertical stacking of multiple chips in the same package offers tremendous advantages in design, test, and ultimate device performance. However, chip stacks have been notoriously expensive to manufacture because all known production techniques occurred at the die level rather than at the wafer level. The primary technical obstacle to mass production of more complicated 3-D vertically integrated packages is the challenge of forming interconnects within the vertical stack. The complexity of stacking chips has limited 3-D packaging to low-volume, very specialized uses, such as military and medical applications, and supercomputers. Wire bonding as a primary 3-D chip-scale packaging technique is limited by the number of chips that can be efficiently stacked, with lengthy links between chips over their edges.

Efforts to further refine 3-D vertically integrated packages continue with the development of a combination of wire-bonding and flip-chip stacking techniques. Although an excellent wafer-level packaging technology, flip chip does not allow for interconnection of more than one IC chip and a substrate. Not surprisingly, chipmakers are being forced to consider cost-effective alternatives and they are placing their collective attention on developing new wafer-level packages (WLPs) and affordable, stacked, wafer-level-packaging (S-WLP) technologies.

3-D stacking

Prior S-WLP attempts were based on the idea of forming holes completely through the wafer, and then somehow depositing insulation and conductive paths inside of these bottomless holes. High-volume production was difficult for bottomless-hole formation by either laser drilling or vacuum plasma etching. The major challenge was in the creation of isolation inside the holes. Other approaches attempted to form isolated buried metal vias from the top-side, grinding off the wafer backside to expose the vias. The problem was the same — how to preserve the isolation on the backside. Backside grinding does not have selective removal rates for different materials, so buried metal vias, isolation, and silicon end up unacceptably close to each other. Here are a few examples.

IBM did some development work using lasers to drill fine holes in brittle materials such as silicon-on-sapphire wafers, and demonstrated the ability to produce holes with diameters down to 12μm in a 325μm-thick wafer with a drill rate of 100–1000 holes/sec. The problem was in metallization of these holes in order to provide through-silicon conductivity.

In an approach developed by LSI Logic, contacts were made on both sides of a silicon device in order to provide more

inputs and outputs. Bottomless holes in the silicon wafer were etched or ion-milled with SiO_2, electrically insulating the walls of each. A conductive plug such as tungsten was deposited in the hole to form the vertical conductor. Despite much effort, this technique was eventually abandoned as not manufacturable.

Toshiba tried to form through-silicon contacts by through-mask-etching the silicon from the backside. The silicon was not insulated in this application. Instead, a gold ball made contact with the front-side metallization. This approach required the use of isotropic and anisotropic through-mask-etching of silicon to form the tapered holes. The major challenges were the alignment of etching on both sides of a wafer and the removal of large amounts of silicon, thus limiting the minimum hole pitch.

Following these unsuccessful attempts, several major companies (including Fujitsu, Hitachi, Matsushita, Mitsubishi, NEC, Oki, Sanyo, Sharp, Sony, Toshiba, IBM Japan, TI Japan, and Rohm) have formed a consortium called the Association of Super-Advanced Electronic Technologies (ASET). One of the primary goals of this consortium is to develop new 3-D, wafer-level-packaging and stacking technologies.

Through-silicon vias

The principal motivation behind the migration of packaging and assembly to the first step in vertical miniaturization — thinner dice (as thin as 50µm) — is obvious: thinner packages. In addition to miniaturization benefits, there are functional benefits of thin dice that include both device performance and reliability. Thinner dice with lower thermal resistance allow high-speed devices to dissipate more heat. Thinner flip-chip dice are more reliable because they can flex within packages so that bonds are not broken. It is now mandatory to thin dice in order to fit chip stacks inside standard-size 3-D packages.

Investment in technologies that provide both wafer-level vertical miniaturization (wafer thinning) and preparation for vertical integration (through-silicon vias) makes good sense. One of the industry's newest technologies, atmospheric downstream plasma (ADP) processing, accomplishes both thinning and opening through-silicon vias in one step. The natural etch-selectivity of the dry ADP chemical process allows for opening isolated buried metal vias to form through-silicon backside contacts during selective maskless etching (backside wafer thinning). Since there is a reduced removal rate of isolation layers compared to silicon, an over-etch will not degrade the isolation.

By removing the arbitrary 2-D conceptual barrier associated with Moore's Law, we can open up a new dimension in ease of design, test, and manufacturing of IC packages. When we need it the most — for portable computing, memory cards, smart cards, cellular telephones, and other uses — we can now follow Moore's Law into the z dimension. ■